Compact DC–60-GHz HJFET MMIC Switches Using Ohmic Electrode-Sharing Technology

Hiroshi Mizutani, *Member, IEEE*, Masahiro Funabashi, Masaaki Kuzuhara, *Member, IEEE*, and Yoichiro Takayama, *Member, IEEE*

***Abstract*—Compact dc–60-GHz heterojunction field-effect transistor (HJFET) monolithic-microwave integrated-circuit (MMIC) switches have been demonstrated for millimeter-wave communications and radar systems. To reduce the MMIC chip size, a novel ohmic electrode-sharing technology (OEST) has been developed for MMIC switches with series–shunt FET configuration. Four FET's of the series–shunt single-pole double-throw (SPDT) MMIC switch were integrated into an area of approximately 0.018 mm^2. The developed MMIC switches have a high power-handling capability with low insertion loss (IL) and high isolation (Iso) at millimeter-wave frequencies. From dc to 60 GHz, the single-pole single-throw (SPST) MMIC switch achieved the IL and Iso of better than 1.64 and 20.6 dB, respectively. At 40 GHz, the IL increases by 1 dB at the input power of 21 dBm. A novel large-signal FET model for the switch circuit is presented. The simulated power-transfer performance shows the excellent agreement with the measured one. The developed MMIC switches will contribute to the low-cost and high-performance millimeter-wave communications and radar systems.**

***Index Terms*— FET's, MMIC switches, modeling, nonlinear circuits.**

I. Introduction

THE development of the millimeter-wave communications and radar systems has increased the need for millimeter-wave switches. In these applications, high-performance and small-size switches suitable for low-cost monolithic-microwave integrated-circuit (MMIC) production are strongly required.

Recently, several millimeter-wave MMIC switches have been reported [1]–[9]. The shunt FET configuration is often used for millimeter-wave-frequency switch circuits [1]–[5]. This configuration is preferred for chip size reduction because of the use of only one FET. However, the shunt FET in the pinched-off state presents a low impedance because it acts as a shunt resistor. Therefore, in the design of the single-pole double-throw (SPDT) switch [in order to obtain low insertion loss (IL) and high isolation (Iso)], a quarter-wavelength transmission line is generally used to transform this low impedance into a high impedance. Due to the use of the quarter-wavelength transformer, SPDT switches employing shunt configuration need a chip size as large as 0.8×2.45 mm^2 for V-band [2], 5.0×2.0 mm^2 for Q-band [5], and 1.27×1.27 mm^2 for K/Ka-band [1]. A series FET configuration with a parallel combined inductor between the source and drain is also available for the millimeter-wave switch circuit [6], [7]. In this configuration, the capacitance of the FET in the pinched-off state and the parallel inductor provides high impedance at the resonant frequency. This configuration has the advantage of obtaining high Iso even at the millimeter-wave frequencies. However, because of its resonated circuit structure, the frequency range which guarantees high impedance is restricted to a narrow bandwidth. Since this resonant frequency is sensitive to changes in the capacitance and inductance, it has poor reproducibility. Furthermore, in the case of millimeter-wave MMIC switches, the inductor externally connected to the FET is generally formed by using a transmission line. The line needs a large space at lower frequencies such as Ka- and V-bands. At the higher frequencies such as W- and D-bands, the line length may be too short to design a practical MMIC switch layout. The series–shunt configuration is often used for millimeter-wave frequency switch circuits [1]. This configuration has the feature of the broad-band switching characteristics. It has the merit that low IL and high Iso may be achieved easily, even at millimeter-wave frequencies. However, this configuration tends to increase the chip size (e.g., to 0.84×1.27 mm^2) because it includes two or more FET's [1]. In this way, a large chip size more than 1 mm^2 has been needed for a millimeter-wave MMIC switch to achieve high switching performance.

In this paper (among these configurations), the series–shunt configuration has been employed for the millimeter-wave switch circuit because it may achieve low IL and high Iso easily, even at millimeter-wave frequencies such as Ka- and V-bands. To reduce the MMIC chip size, a novel ohmic electrode-sharing technology (OEST) has been developed [12]. The implemented millimeter-wave MMIC switches using OEST with extremely reduced chip size and broad-band excellent switching performance will be reported. The design consideration of a millimeter-wave single-pole single-throw (SPST) MMIC switch with the series–shunt FET configuration using the novel OEST will be described first. The most effective application of the OEST for the SPDT MMIC switch design will be demonstrated second. The MMIC fabrication process and MMIC performance will be presented third. Finally, the novel large-signal FET model for the switch circuit will be proposed and large-signal operation will be discussed.

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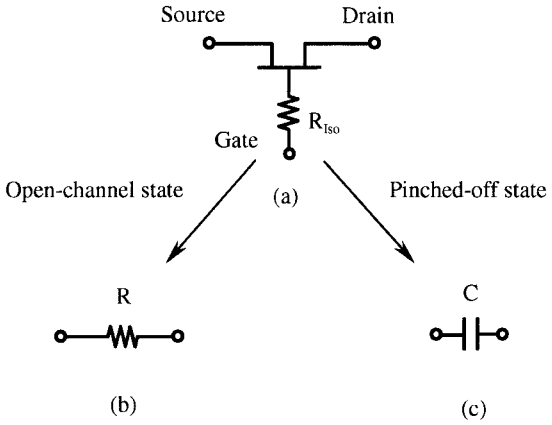

Fig. 1. (a) Simple FET model for switch circuit. (b) Open-channel state. (c) Pinched-off state.

II. Circuit Design

In this section, the circuit-design concept of the SPST MMIC switch is described. In the small-signal design of the millimeter-wave MMIC switch, a choice of an active device, layout technique, and optimal FET gatewidths are essential for high performance. Moreover, in the large-signal operation, the source grounded drain current, drain breakdown voltage, gate bias voltage, and threshold voltage are also important parameters for high power-handling capability of the MMIC switch, as discussed in detail in Section VI.

A. Small-Signal Design

1) Choice of Active Device: In the switch circuit, an FET is almost equivalent to a two-port device when an Iso resistor $R_{\rm Iso}$ with sufficiently large resistance is inserted into the gate bias circuit, as shown in Fig. 1(a). An equivalent circuit of the FET in the open-channel state is a simple resistor, as shown in Fig. 1(b). In the pinched-off state, the resistor is replaced by a simple capacitor, as shown in Fig. 1(c). Thus, in the series–shunt configuration, shown in Fig. 2(a), the switch circuit in the on-state is shown in Fig. 2(b) as a series resistor R, in conjunction with a shunt capacitor C, where $C_{\rm ps}$ and $C_{\rm pd}$ are the parasitic capacitances, which will be mentioned later. The switch in the off-state is expressed as the combination of a series capacitor and a shunt resistor, as shown in Fig. 2(c). It is important for achieving the lower IL and higher Iso that the resistance and capacitance of the FET's in the series–shunt configuration switch circuit are kept as small as possible.

The heterojunction field-effect transistor (HJFET) with 0.15-μm gate length for the millimeter-wave applications provides as small resistance and capacitance as 7 Ω and 20 fF for the gatewidths of 100 μm, respectively [11]. This HJFET technology was used for the millimeter-wave MMIC switches.

2) Effect of OEST: The connection line between series- and shunt-FET's arranged apart from each other would result in the impedance mismatch and transmission loss at higher frequencies such as millimeter waves. Two-source and two-drain ohmic electrodes separately formed need the excessive large area more than the net area of four electrodes for forming the switch component. Furthermore, these ohmic

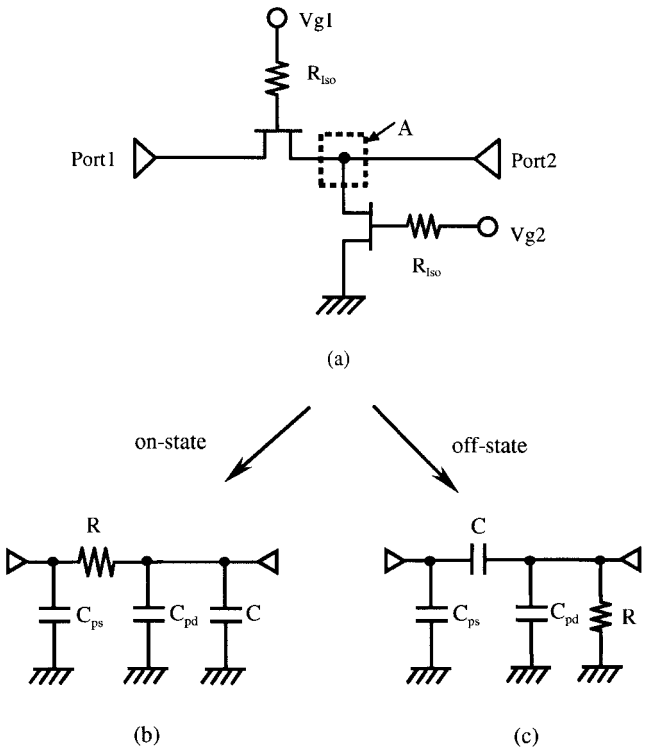

Fig. 2. (a) Schematic diagram of SPST switch circuit. (b) Equivalent circuit taking account of parasitic capacitance in on- and (c) off-states.

electrodes induce the parasitic capacitances $C_{\rm ps}$ and $C_{\rm pd}$ between each electrode and the backside grounded metal. These parasitic capacitances degrade the IL characteristics. In [12], the novel OEST has been developed and the feasibility of the OEST has been demonstrated. In the OEST, two ohmic electrodes of two FET's with the same electric potential in the design-circuit share of only one ohmic electrode. By introducing the OEST, the impedance mismatch and transmission loss between series- and shunt-FET's will not occur. Moreover, the parasitic capacitances will be reduced to 3/4 of the conventional layout capacitances, so that high performance can be expected. Also, the small chip size will realize low-cost MMIC's. Actually, by employing the OEST, the switch component area not including interconnecting lines and bonding pads can be reduced to approximately 1/3 of the conventional switch component area [1].

3) Optimal Gatewidths: The small-signal design of the SPST and the SPDT switch circuits with the series–shunt configuration has been executed based on the above-mentioned study. The series FET's are controlled with gate bias V_{g1}, and the shunt FET's with V_{g2}. In the on-state, the control gate-voltages V_{g1} and V_{g2} are 0 and -5 V, respectively. In the off-state, the above bias condition is exchanged. In this circuit, the Iso resistors of some kilo ohms were inserted into each gate bias line. Then, by taking account of the parasitic capacitances, the equivalent SPST switch circuits in the on- and off-states are shown in Fig. 2(b) and (c). Thus, the IL and Iso are expressed as (1) and (2), shown at the bottom of the following page, where R and C are the resistance in the open-channel state FET and the capacitance in the pinched-off state FET, respectively. ω is the angular frequency and Z_0 is

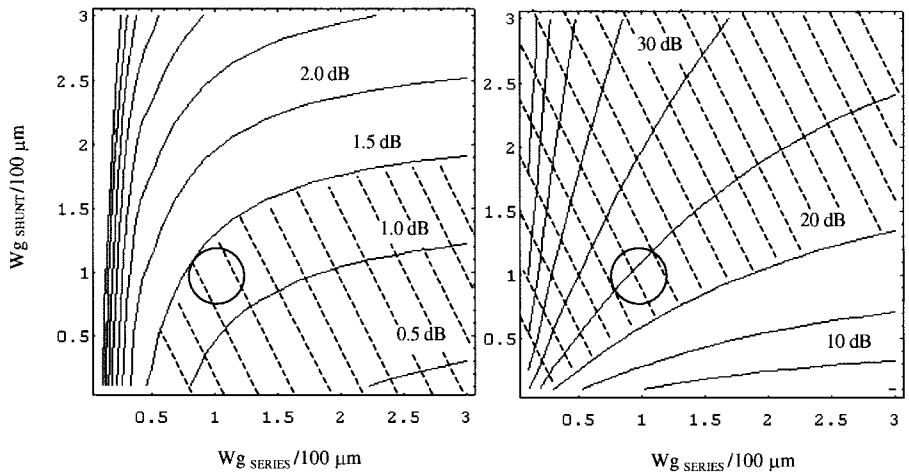

Fig. 3. Contour maps for (a) IL and (b) Iso, with respect to series- and shunt-gatewidths.

the characteristic impedance of the connected ports. Also, $C_{\rm ps}$ and $C_{\rm pd}$ are the source and drain parasitic capacitances in the pinched-off state, respectively. For 100-μm gatewidth, R is 7 Ω and C is 20 fF. $C_{\rm ps}$ and $C_{\rm pd}$ are both 10 fF. These design parameters were determined by extraction from our standard HJFET for millimeter-wave applications [12].

The gatewidths of the HJFET's used for the series–shunt configuration switch are determined so as to provide the optimal performance of low IL and high Iso at millimeter-wave frequencies such as 60 GHz by using (1) and (2). If the gatewidths are multiplied by k, the resistance is $1/k$ times of the unit resistance R_0 for the unit gatewidth and the capacitance is k times of the unit capacitance C_0. The optimal gatewidths are determined for providing acceptable IL and Iso. The contour maps of the IL and Iso with respect to gatewidths, calculated from (1) and (2) at 60 GHz, are shown in Fig. 3(a) and (b), respectively. The specification of the MMIC switch has been set as the IL of less than 1.5 dB and the Iso of more than 20 dB at 60 GHz. In the figure, each axis represents normalized gatewidth k of the shunt FET and the series FET, respectively, and the unit gatewidth is 100 μm. From Fig. 3(a) and (b), the optimal normalized gatewidths for both series- and shunt-FET's satisfying the above specification are around $k = 1.0$, which are marked by circles. Thus, the optimal gatewidths are determined as 100 μm for both series- and shunt-FET's.

The SPDT switch circuit is shown in Fig. 4. This SPDT switch has the previous SPST switches for each branch. By applying V_{g1} and V_{g2} biases (mentioned above or vice versa), a input signal to Port 1 may be switched to Ports 2 or 3 The

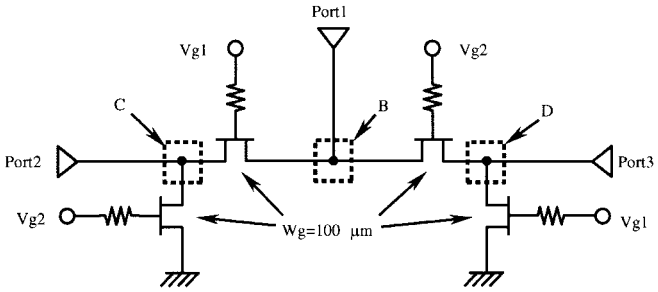

Fig. 4. Schematic diagram of SPDT switch circuit.

calculated frequency responses of the IL and Iso are described in Section V. They indicate good agreement with the measured data, as explained later.

B. Large-Signal Consideration

Atwater *et al.* [13] have suggested that the maximum power for the switching operation would be expressed by the FET parameters, such as the saturation drain current at $V_{\rm gs} = 0$ V and the drain breakdown voltage in the pinched-off state. However, in the large-signal operation, the drain voltage swings to the negative region. Therefore, it is also important to take the negative drain voltage region into account. As shown later, higher saturation drain current at $V_{\rm gs} = 0$ V, higher drain breakdown voltage, higher threshold voltage, and lower gate bias voltage are required to realize high power-handling capability of the MMIC switch. These parameters can be improved by modifying the FET structure such as the epitaxial layer structure and the gate recess structure. Therefore, in the

$$\mathrm{IL} = 10\log\frac{4}{\left\{2+\frac{R}{Z_0}-\omega^2 Z_0 R C_{\rm ps}(C_{\rm pd}+C)\right\}^2+\left\{\omega(R+Z_0)(C_{\rm ps}+C_{\rm pd}+C)\right\}^2} \tag{1}$$

$$\mathrm{Iso} = 10\log\frac{4}{\left\{2+\frac{C_{\rm ps}+C_{\rm pd}}{C}+\frac{Z_0}{R}\left(1+\frac{C_{\rm ps}}{C}\right)\right\}^2+\left\{\omega Z_0\left(C_{\rm ps}+C_{\rm pd}+\frac{C_{\rm ps}C_{\rm pd}}{C}\right)-\frac{1}{\omega C}\left(\frac{1}{R}+\frac{1}{Z_0}\right)\right\}^2} \tag{2}$$

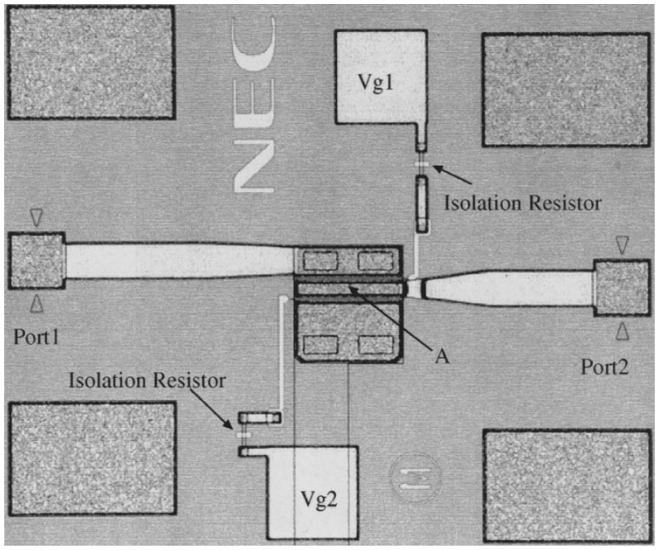

Fig. 5. Top view of SPST MMIC switch.

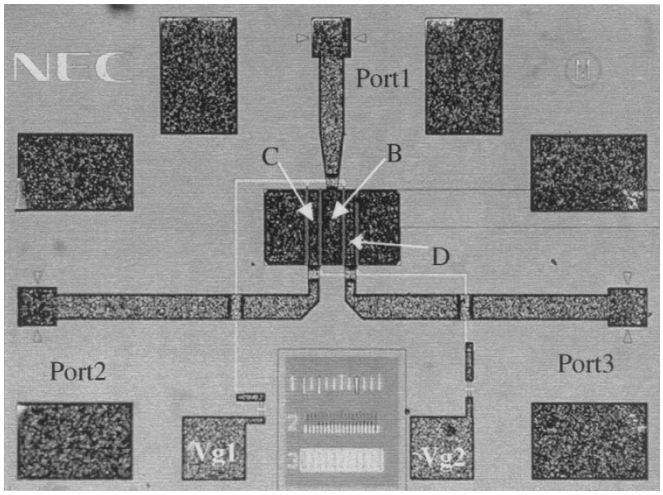

Fig. 6. Top view of SPDT MMIC switch.

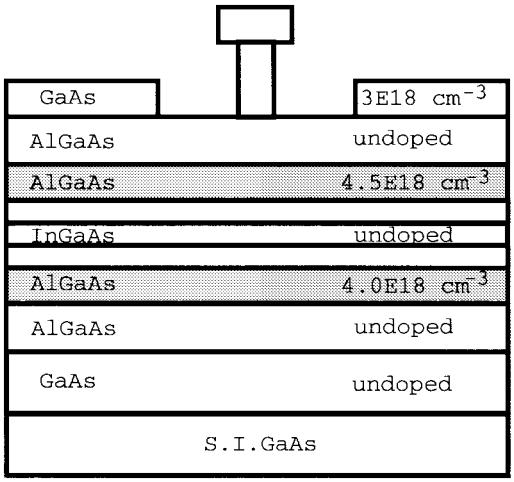

Fig. 7. Cross-sectional view of an HJFET used for MMIC switches.

design of the HJFET structure, the epitaxial layer structure and the gate recess structure were designed so that the MMIC switch can exhibit high current-handling capability as well as high breakdown voltages.

III. MMIC Layout Design

In the conventional layout design, the FET's of the series–shunt configuration are interconnected by transmission lines [1]. Consequently, the large switch component area is needed. In this paper, by employing the OEST, no interconnecting lines are inserted between the series- and the shunt-FET's because an ohmic electrode is shared by the source of one FET and drain of the other FET. The top view of the SPST MMIC switch using the OEST is shown in Fig. 5. In Fig. 2(a), the OEST is applied to the part marked by the dotted rectangle. The OEST area in Fig. 5 is labeled A, which corresponds to the same label in Fig. 2(a). The ohmic electrode labeled A is shared by the source of the series FET and drain of the shunt FET. The source of the shunt FET is grounded through the via holes. Two FET's and via holes for the SPST switch component of the series–shunt configuration are integrated into a very small area of 0.10×0.11 mm^2. Total chip size including bonding pad areas is 0.52×0.63 mm^2.

Using the OEST, the more effective size reduction is expected for the application to the SPDT MMIC switch. Fig. 6 shows the top view of the SPDT MMIC switch. The OEST areas are labeled B, C, and D, which correspond to the same labels in Fig. 4. The ohmic electrode labeled B is the drain ohmic electrode shared by two series FET's attached to each branch. The ohmic electrodes labeled C and D are shared by the source or the drain of the series FET and the drain of the shunt FET in each branch. The sources of the shunt FET's are grounded through the via holes. The four FET's with two via holes, which compose the SPDT switch with the series–shunt configuration, are integrated into a very small lumped area of 0.1×0.18 mm^2. Total chip size including bonding pad areas is 0.86×0.64 mm^2. This is about 1/2 of the MMIC chip area which has been reported in [1]. In this way, the OEST could successfully reduce the switch component area and the MMIC chip size.

IV. MMIC Fabrication

The MMIC's were fabricated using a 0.15-μm T-shaped gate HJFET MMIC process for millimeter-wave applications with high reliability [10], [11]. Fig. 7 shows a cross-sectional view of the HJFET. A double heterojunction structure was employed to achieve high drain current and high breakdown voltage. N-type AlGaAs carrier supply layers are placed both above and below the undoped InGaAs channel layer. The typical FET has the maximum drain current of 600 mA/mm with a threshold voltage of -2 V, and a reverse gate breakdown voltage of more than 10 V. f_T and $f_{\max}$ are more than 50 and 180 GHz, respectively. The Iso resistors were monolithically fabricated using the same epitaxial layers used for FET's, which were implemented by partially removing the top layer for the ohmic contacts by a selective wet-etching technique.

V. MMIC Performance

The small-signal scattering characteristics of the developed switches were measured from dc to 62.5 GHz. The frequency responses of the IL, Iso and return loss of the SPST switch are

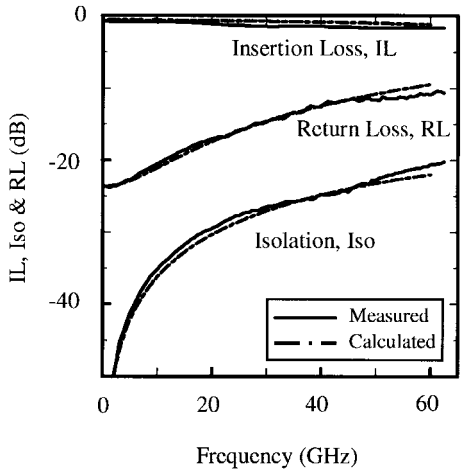

Fig. 8. IL, Iso, and return loss of SPST MMIC switch. The control gate–voltage are 0 and −5 V for the open-channel and pinched-off states, respectively.

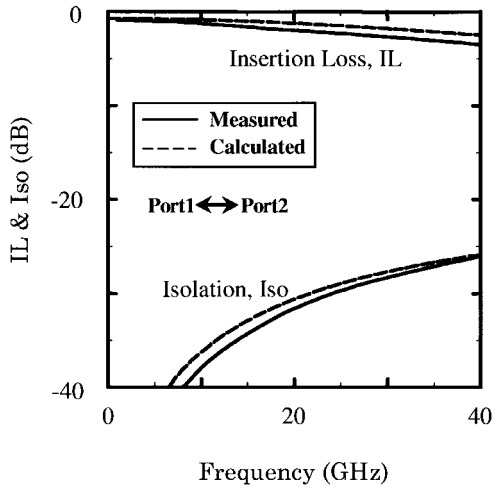

Fig. 9. IL, Iso, and return loss of SPDT MMIC switch. The control gate-voltage are 0 and −5 V for the open-channel and pinched-off states, respectively.

shown in Fig. 8, together with modeled performance described in Section II. These IL and Iso curves show an excellent ON/OFF ratio from dc to 62.5 GHz due to employing the series–shunt configuration. The ON/OFF ratio is more than 20 dB up to 55 GHz. From dc to 60 GHz, the IL is better than 1.64 dB and the Iso is better than 20.6 dB. The return loss is better than 10 dB through the measured frequencies. The measured results show an excellent agreement with the calculated results.

The measured and calculated small-signal scattering characteristics of the SPDT MMIC switch are shown in Fig. 9. Terminating one output port (Port 3 in Fig. 4) to 50 Ω, the IL and Iso were measured between the remaining ports (Ports 1 and 2 in Fig. 4). At 40 GHz, the measured IL and Iso are 3.5 and 25.5 dB, respectively. The measured curves shows a good agreement with the calculated curves.

The measured power-handling capability of the SPST MMIC switch at 40 GHz is shown in Fig. 10 by solid lines. The IL remains almost constant up to 20-dBm input power. The ON/OFF ratio is better than 20 dB up to 18-dBm input power. The IL increases by 1 dB at 21-dBm input power. The input power capability is about twice as large as that of the conventional SPDT MMIC switch using almost the same-size GaAs MESFET's in the series–shunt configuration [1].

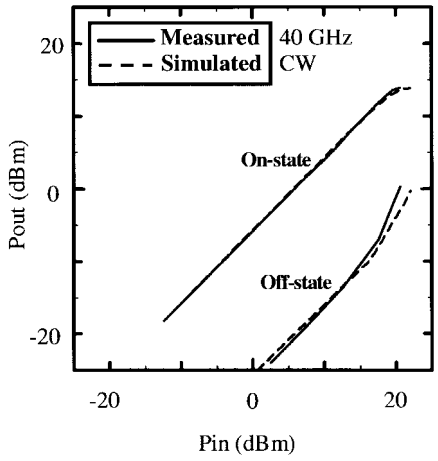

Fig. 10. Power-handling capability of SPST switch at 40 GHz. The control gate–voltage are 0 and −5 V for the open-channel and pinched-off states, respectively.

VI. Discussion of Large-Signal Modeling

In this section, the large-signal operation of the switch circuit is discussed. A novel large-signal FET model for the switch circuit is also presented. In the model, the FET can be equivalently expressed as the parallel combination of the capacitor and current source, as shown in Fig. 11. The model is based on the symbolical defined model in the HP Microwave Design System.[1] To study the feasibility of this two-port model easily, a simple hyperbolic tangent current model is newly employed. That is, in the open-channel state, the drain current is described as (3)–(7), shown at the bottom of this page. In the pinched-off state, the drain current is as shown in (8)–(13), at the bottom of the following page,

[1] See HP Microwave Design System, Component Catalog, vol. 4, p. 5-5.

$$I_{\mathrm{ds}_O} = \begin{cases} \beta\left(-R_{\mathrm{Iso}} I_{g_O} + \phi_B - V_T\right)^2 \tanh(\alpha V_{\mathrm{ds}}), & V_{\mathrm{ds}} \le -\phi_B \quad (3) \\ \beta\left(V_{\mathrm{gs}_O} - V_{\mathrm{ds}} - V_T\right)^2 \tanh(\alpha V_{\mathrm{ds}}), & -\phi_B \le V_{\mathrm{ds}} \le 0 \quad (4) \\ \beta\left(V_{\mathrm{gs}_O} - V_T\right)^2 \tanh(\gamma V_{\mathrm{ds}}), & 0 \le V_{\mathrm{ds}} \quad (5) \end{cases}$$

$$I_{g_O} = \begin{cases} 0, & -\phi_B \le V_{\mathrm{ds}} \quad (6) \\ I_{s_G}\left\{\exp\left[\kappa_f\left(V_{\mathrm{gs}_O} - V_{\mathrm{ds}} - \phi_B\right)\right] - 1\right\}, & V_{\mathrm{ds}} \le -\phi_B \quad (7) \end{cases}$$

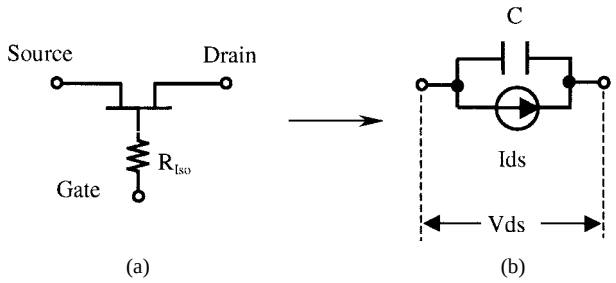

Fig. 11. Two-port large-signal FET model for switch circuit.

TABLE I
PARAMETER VALUES FOR LARGE-SIGNAL SIMULATION

ϕ_B	0.31 V
α	2.0 V^{-1}
β	0.02 A/V^2
γ	1.5 V^{-1}
κ_f	0.01 V^{-1}
κ_r	1.0 V^{-1}
V_T	−1.5 V
R_{Iso}	100 kΩ
Is_G	0.00007 A
Is_D	0.1 A
V_B	7.3 V
Vgs_O	0 V
Vgs_P	−5.0 V

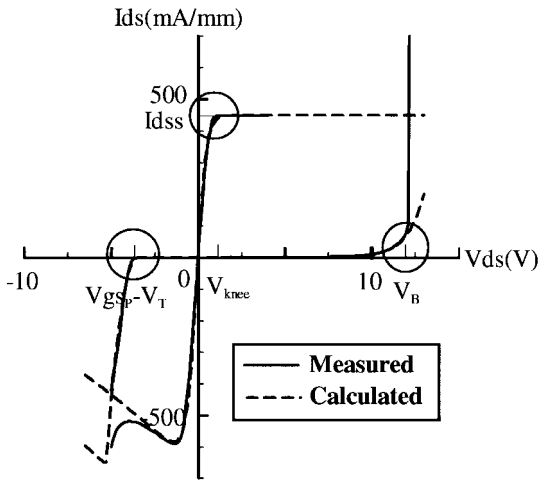

Fig. 12. Current–voltage characteristics of FET switch.

where β is the transconductance parameter, ϕ_B is the build-in potential, V_T is the threshold voltage, I_{s_G} is the gate forward current parameter and I_{s_D} is the drain breakdown current parameter, I_{g_o} is the forward-biased gate current and I_{g_P} is the reverse-gate breakdown current, V_{gs_O} and V_{gs_P} are the gate–source voltages for the open-channel and pinched-off states, respectively, and V_B is the drain breakdown voltage in the pinched-off state. α, γ, κ_f, and κ_r are the voltage scaling factors. In the practical operation of the series FET in Fig. 2(a), the gate–source voltage varies with respect to the time. In this model, for simple analysis, V_{gs_O} and V_{gs_P} are assumed to be equal to the control gate–voltages for the open-channel and pinched-off states, respectively. The parameter values used for simulation are given in Table I. In Fig. 10, the broken lines are harmonic-balance simulation results using the novel two-port current–voltage model represented by (3)–(13). The measured and simulated curves are in good agreement for both the on- and off-states. On this current model, the current–voltage characteristics for both the open-channel and pinched-off states are shown in Fig. 12. The input voltage/current swing will be limited at the points marked by circles. That is, for the pinched-off state, the voltage will be limited at the drain voltage corresponding to the threshold voltage of the negative biased drain $V_{\mathrm{gs}_P} - V_T$ or the drain breakdown voltage V_B. In the case of $V_{\mathrm{gs}_P} = -5$ V, $V_{\mathrm{gs}_P} - V_T$ limits the voltage swing in the pinched-off state. For the open-channel state, the current will be limited at the knee voltage $V_{\mathrm{knee}} = 1/\gamma$ corresponding to the saturation drain current at $V_{\mathrm{gs}_O} = 0$ V, $I_{\mathrm{dss}} = \beta V_T^2$.

On the other hand, the capacitance parallel combined to the current source C consists of the series combination of the gate–source capacitance C_{gs} and the gate–drain capacitance C_{gd}. C_{gs} and C_{gd} change with both the gate–source and the drain–source voltages V_{gs} and V_{ds}. For both open-channel and pinched-off states, the electrical cross-sectional configuration of the cold FET with zero drain bias is symmetrical with respect to the gate electrode. Besides, when the drain voltage increases under some constant gate voltage, the electrical cross-sectional configuration is asymmetrical with respect to the gate electrode. That is, C_{gd} decreases with a V_{ds} increase. Therefore, C decreases monotonically with respect to V_{ds}. As a result, the source–drain capacitance of the FET indicates the maximum value when the FET is cold for both the open-channel and pinched-off states. The variation of the capacitance with respect to the input voltage swing do not cause the degradation of both the IL and Iso of the FET switch. In other words, the large-signal operation of the FET switch can be evaluated with only the previous current model. In the reported switch [1], the degradation of the IL and Iso were caused by current limiting in the series FET and shunt FET, respectively. From the presented model, it is found that the voltage swing is clipped at the series FET for both on- and

$$I_{\mathrm{ds}_P} = \begin{cases} \beta\left(-R_{\mathrm{Iso}} I_{g_P} + \phi_B - V_T\right)^2 \tanh(\alpha V_{\mathrm{ds}}), & V_{\mathrm{ds}} \le V_{\mathrm{gs}_P} - \phi_B \quad (8) \\ \beta\left(V_{\mathrm{gs}_P} - V_{\mathrm{ds}} - V_T\right)^2 \tanh(\alpha V_{\mathrm{ds}}), & V_{\mathrm{gs}_P} - \phi_B \le V_{\mathrm{ds}} \le V_{\mathrm{gs}_P} - V_T \quad (9) \\ 0, & V_{\mathrm{gs}_P} - V_T \le V_{\mathrm{ds}} \le V_B \quad (10) \\ I_{s_D}\{\exp[\kappa_r(V_{\mathrm{ds}} - V_B)] - 1\}, & V_B \le V_{\mathrm{ds}} \quad (11) \end{cases}$$

$$I_{g_P} = \begin{cases} 0, & V_{\mathrm{gs}_P} - \phi_B \le V_{\mathrm{ds}} \quad (12) \\ I_{s_G}\left\{\exp\left[\kappa_f\left(V_{\mathrm{gs}_P} - V_{\mathrm{ds}} - \phi_B\right)\right] - 1\right\}, & V_{\mathrm{ds}} \le V_{\mathrm{gs}_P} - \phi_B \quad (13) \end{cases}$$

off-states. The voltage swing is limited at V_{knee} and $V_{\text{gs}_P} - V_T$ for on- and off-state, respectively.

VII. Summary

Compact HJFET MMIC switches with high performance have been developed for millimeter-wave applications. A novel OEST for reducing MMIC switch chip size has realized the series–shunt FET's with a reduced area of approximately 0.018 mm^2 for an SPDT MMIC switch. The developed MMIC switches have shown excellent switching performance at the millimeter-wave frequencies. The novel large-signal FET model for describing the power-handling capability has been provided, and it has been shown that the model can predict the measured power-transfer characteristics at millimeter waves.

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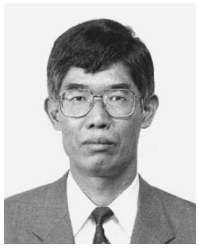

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